HITACHI
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Hard Disk Drive Specification

Deskstar 7K250

3.5 inch Serial ATA hard disk drive

Models:

HDS722540VLSA80
HDS722580VLSA80
HDS722512VLSA80
HDS722516VLSA80
HDS722525VLSA80

Version 1.6

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Table of Contents

List of Tables

1.0 General

1.1 Introduction

This document describes the specifications of the Deskstar 7K250, a 3.5-inch hard disk drive with Serial ATA interface and a rotational speed of 7200 RPM.

HDS722540VLSA80	41.1 GB
HDS722580VLSA80	82.3 GB
HDS722512VLSA80	123.5 GB
HDS722516VLSA80	164.7 GB
HDS722525VLSA80	257.3 GB

These specifications are subject to change without notice.

1.2 References

- Information Technology - AT Attachment with Packet Interface-6.

1.3 Abbreviations

Abbreviation	Meaning
A	Ampere
AC	alternating current
AT	Advanced Technology
ATA	Advanced Technology Attachment
BIOS	Basic Input/Output System
C	Celsius
CSA	Canadian Standards Association
C-UL	Canadian-Underwriters Laboratory
Cyl	cylinder
DC	Direct Current
DFT	Drive Fitness Test
DMA	Direct Memory Access
ECC	error correction code
EEC	European Economic Community
EMC	electromagnetic compatibility
ERP	Error Recovery Procedure
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
FRU	field replacement unit
G	gravity (a unit of force)

G^2/Hz	$(32\ ft/sec)^2$ per Hertz
Gb	1,000,000,000 bits
GB	1,000,000,000 bytes
GND	ground
h	hexadecimal
HDD	hard disk drive
Hz	Hertz
I	Input
ILS	integrated lead suspension
I/O	Input/Output
ISO	International Standards Organization
KB	1,000 bytes
Kbpi	1000 bits per inch
kgf-cm	kilogram (force)-centimeter
KHz	kilohertz
LBA	logical block addressing
Lw	unit of A-weighted sound power
m	meter
max	maximum
MB	1,000,000 bytes
Mbps	1,000,000 bits per second
MHz	megahertz
MLC	Machine Level Control
mm	millimeter
ms	millisecond
us, ms	microsecond
O	Output
OD	Open Drain Programmed Input/Output
PIO	
POH	power on hours
Pop	population
P/N	part number
p-p	peak-to-peak
PSD	power spectral density
RES	radiated electromagnetic susceptibility
RFI	radio frequency interference
RH	relative humidity
RMS	root mean square
RPM	revolutions per minute
RST	reset
R/W	read/write
sec	second
SELV	secondary low voltage

S.M.A.R.T	Self-Monitoring, Analysis, and Reporting Technology
TPI	tracks per inch
Trk	track
TTL	transistor-transistor logic
UL	Underwriters Laboratory
V	volt
VDE	Verband Deutscher Electrotechniker
W	watt
3-state	transistor-transistor tristate logic

1.4 Caution

- Do not apply force to the top cover.
- Do not cover the breathing hole on the top cover.
- Do not touch the interface connector pins or the surface of the printed circuit board
- This drive can be damaged by electrostatic discharge (ESD). Any damages incurred to the drive after its removal from the shipping package and the ESD protective bag are the responsibility of the user.

2.0 General features of the drive

- Formatted capacities of 40 GB - 250 GB
- Spindle speeds of 7200 RPM
- Fluid Dynamic Bearing motor
- Enhanced IDE interface
- Sector format of 512 bytes/sector
- Closed-loop actuator servo
- Load/Unload mechanism, non head disk contact start/stop
- Automatic Actuator lock
- Interleave factor 1:1
- Seek time of 8.5 ms (30-GB, 40-GB, and 60-GB models), 8.2 ms (all other models) typical without Command Overhead)
- Sector Buffer size of 8192 KB (Upper 260 KB is used for firmware)
- Ring buffer implementation
- Write Cache
- Queued feature support
- Advanced ECC On The Fly (EOF)
- Automatic Error Recovery procedures for read and write commands
- Self Diagnostics on Power on and resident diagnostics
- Serial Data Transfer 1.5 Gb/sec
- CHS and LBA mode
- Power saving modes/Low RPM idle mode (APM)
- S.M.A.R.T. (Self Monitoring and Analysis Reporting Technology)
- Support security feature
- Quiet Seek mode (AAM)
- 48-bit addressing feature

Part 1. Functional specification

3.0 Fixed-disk subsystem description

3.1 Control electronics

The drive is electronically controlled by a microprocessor, several logic modules, digital/analog modules, and various drivers and receivers. The control electronics performs the following major functions:

- Controls and interprets all interface signals between the host controller and the drive.
- Controls read write accessing of the disk media, including defect management and error recovery.
- Controls starting, stopping, and monitoring of the spindle.
- Conducts a power-up sequence and calibrates the servo.
- Analyzes servo signals to provide closed loop control. These include position error signal and estimated velocity.
- Monitors the actuator position and determines the target track for a seek operation.
- Controls the voice coil motor driver to align the actuator in a desired position.
- Constantly monitors error conditions of the servo and takes corresponding action if an error occurs.
- Monitors various timers such as head settle and servo failure.
- Performs self-checkout (diagnostics).

3.2 Head disk assembly

The head disk assembly (HDA) is assembled in a clean room environment and contains the disks and actuator assembly. Air is constantly circulated and filtered when the drive is operational. Venting of the HDA is accomplished via a breather filter.

The spindle is driven directly by an in-hub, brushless, sensorless DC drive motor. Dynamic braking is used to quickly stop the spindle.

3.3 Actuator

The read/write heads are mounted in the actuator. The actuator is a swing-arm assembly driven by a voice coil motor. A closed-loop positioning servo controls the movement of the actuator. An embedded servo pattern supplies feedback to the positioning servo to keep the read/write heads centered over the desired track.

The actuator assembly is balanced to allow vertical or horizontal mounting without adjustment.

When the drive is powered off, the actuator automatically moves the head to the actuator ramp outside of the disk where it parks.

4.0 Drive characteristics

4.1 Formatted capacity

Table 1: Formatted capacities

	HDS722540VLSA80	HDS722580VLSA80	HDS722512VLSA80
Physical Layout			
Label capacity (GB)	40	80	120
Bytes per sector	512	512	512
Sectors per track	567-1170	567-1170	567-1170
Number of heads	1	2	3
Number of disks	1	1	2
Data sectors per cylinder	567-1170	1134-2340	1701-3510
Data cylinders per zone	1444-4501 (90KTPI) 100-6846 (87KTPI)	1444-4501 (90KTPI) 100-6846 (87KTPI)	1444-4501
Logical layout[1]			
Number of heads	16	16	16
Number of Sectors per track	63	63	63
Number of Cylinders[2]	16,383	16,383	16,383
Number of sectors	80,418,240	160,836,480	241,254,720
Total logical data bytes	41,174,138,880	82,348,277,760	123,522,416,640

	HDS722516VLSA80	HDS722525VLSA80
Physical Layout		
Label capacity (GB)	160	250
Bytes per sector	512	512
Sectors per track	567-1170	567-1170
Number of heads	4	6
Number of disks	2	3
Data sectors per cylinder	2268-4680	3402-7020
Data cylinders per zone	1444-4501	1500-5000
Logical layout[1]		
Number of heads	16	16
Number of Sectors per track	63	63
Number of Cylinders[2]	16,383	16,383
Number of sectors	321,672,960	488,397,168
Total logical data bytes	164,696,555,520	250,059,350,016

Notes:

[1.] Number of cylinders: For drives with capacities greater than 8.45 GB the Identify Device information word 01 limits the number of cylinders to 16, 383 per the ATA specification.

[2.] Logical layout: Logical layout is an imaginary drive parameter (that is, the number of heads) which is used to access the drive from the system interface. The logical layout to Physical layout (that is, the actual Head and Sectors) translation is done automatically in the drive. The default setting can be obtained by issuing an IDENTIFY DEVICE command.

4.2 Data sheet

Table 2: Mechanical positioning performance

Data transfer rates (Mbps)	757
Interface transfer rates (Mb/s)	100
Data buffer size[1] (KB)	8192
Rotational speed (RPM)	7200
Number of buffer segments (read)	up to 128
Number of buffer segments (write)	up to 63
Recording density - max (Kbpi)	689
Track density [TPI]	87/90 (40/80GB) 90 (120/160GB) 90/93.5 (250GB)
Areal density - max (Gbits/in^2)	62
Number of data bands	30

Notes:

[1]Upper 254 KB is used for firmware

[2]Mechanical positioning performance

4.3 Drive organization

4.3.1 Drive format

Upon shipment from manufacturing the drive satisfies the sector continuity in the physical format by means of the defect flagging strategy described in Section 5.0, “Defect flagging strategy” on page 21 in order to provide the maximum performance to users.

4.3.2 Cylinder allocation

Table 3: Cylinder allocation

Zone	Physical cylinders			Blk/Trk
	87KTPI	90KTPI	93.5KTPI	
0	6,846	1,444	1,500	1,170
1	4,445	3,095	4,400	1,147
2	1,445	3,095	4,400	1,147
3	2,326	3,389	3,961	1,134
4	2,299	3,043	3,396	1,125
5	6,587	3,845	5,000	1,080
6	6,087	3,946	5,000	1,080
7	5,611	4,501	3,800	1,026
8	2,111	4,001	3,800	1,026
9	1,465	3,232	3,112	1,012
10	2,508	3,726	3,663	990
11	2,526	3,193	2,070	972
12	4,030	4,286	2,868	945
13	3,822	3,120	3,033	918
14	2,797	4,037	3,006	900
15	2,039	4,073	2,728	877
16	2,242	4,037	2,947	855
17	3,434	4,073	3,400	810
18	3,434	3,573	3,400	810
19	2,666	3,276	3,400	742
20	2,667	2,675	3,400	742
21	2,504	2,408	3,229	720
22	1,702	1,960	1,829	702
23	1,499	1,568	2,150	675
24	1,499	1,568	2,150	675
25	2,096	2,082	2,283	630

Table 3: Cylinder allocation

26	1,546	2,157	2,285	630
27	1,500	1,700	1,748	607
28	1,000	1,570	1,700	594
29	1,056	1,521	2,100	567

Physical cylinder is calculated from the starting data track of 0. It is not relevant to logical CHS. Depending on the capacity some of the inner zone cylinders are not allocated.

Data cylinder

This cylinder contains the user data which can be sent and retrieved via read/write commands and a spare area for reassigned data.

Spare cylinder

The spare cylinder is used by Hitachi Global Storage Technologies manufacturing and includes data sent from a defect location.

4.4 Performance characteristics

Drive performance is characterized by the following parameters:

- Command overhead
- Mechanical head positioning
  - Seek time
  - Latency
- Data transfer speed
- Buffering operation (Look ahead/Write cache)

All the above parameters contribute to drive performance. There are other parameters that contribute to the performance of the actual system. This specification tries to define the bare drive characteristics, not system throughput, which depends on the system and the application.

4.4.1 Command overhead

Command overhead is defined as the time required from the time the command is written into the command register by a host to the assertion of DRQ for the first data byte of a READ command when the requested data is not in the buffer excluding Physical seek time and Latency.

The table below gives average command overhead.

Table 4: Command overhead

Command type (Drive is in quiescent state)	Time (typical) (ms)	Time (typical) for queued command (ms)
Read (cache not hit) (from Command Write to Seek Start)	0.5	0.5
Read (cache hit) (from Command Write to DRQ)	0.1	0.1
Write (from Command Write to DRQ)	0.015	0.05
Seek (from Command Write to Seek Start)	0.5	not applicable

4.4.2 Mechanical positioning

4.4.2.1 Average seek time (including settling)

Table 5: Mechanical positioning performance

Command type		Typical (ms)	Max (ms)
Read	120-250GB	8.2	9.2
	40-80GB	8.5	9.5
Write	120-250GB	9.2	10.2
	40-80GB	9.5	10.5
Read (Quiet Seek mode)		19.5	20.5
Write (Quiet Seek mode)		20.5	21.5

The terms “Typical” and “Max” are used throughout this document and are defined as follows:

Typical The average of the drive population tested at nominal environmental and voltage conditions.

Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See Section 6.2, “Environment” on page 27 and Section 6.3, “DC power requirements” on page 29 for ranges.)

The seek time is measured from the start of the actuator’s motion to the start of a reliable read or write operation. A reliable read or write implies that error correction or recovery is not used to correct arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{max} (m10\ n)(Tnin + Tnout)}{(max + 1)(max)}$$

where

max = Maximum seek length
n = Seek length (1 to max)
Tnin = Inward measured seek time for an n track seek
Tnout = Outward measured seek time for an n track seek

4.4.2.2 Full stroke seek time (without command overhead, including settling)

Table 6: Full stroke seek time

Function		Typical (ms)	Max (ms)
Read	120-250GB	14.7	17.7
	40-80GB	15.1	18.1
Write	120-250GB	15.7	18.7
	40-80GB	16.1	19.1
Read (Quiet Seek mode)		32.5	35.5
Write (Quiet Seek mode)		33.5	36.5

Full stroke seek is measured as the average of 1,000 full stroke seeks with a random head switch from both directions (inward and outward).

4.4.2.3 Head switch time (head skew)

Table 7: Head switch time

	Head switch time-typical (ms)
87/90/93.5 KTPI	1.4

Head switch time is defined as the amount of time required by the fixed disk to complete a seek of the next sequential track after reading the last sector in the current track

The measuring method is given in 4.4.5, “Throughput” on page 19.

4.4.2.4 Cylinder switch time (cylinder skew)

	Cylinder Switch time - typical (ms)
87/90/93.5 KTPI	1.7

Cylinder switch time is defined as the amount of time required by the fixed disk to access the next sequential block after reading the last sector in the current cylinder.

The measuring method is given in Section 4.4.5, “Throughput” on page 19.

4.4.2.5 Single track seek time (without command overhead, including settling)

Table 8: Single track seek time

Function	Typical (ms)	Max (ms)
Read	0.8	1.5
Write	1.3	2.0
Read (Quiet Seek mode)	0.8	1.5
Write (Quiet Seek mode)	1.3	2.0

Single track seek is measured as the average of one (1) single track seek from every track in both directions (inward and outward).

4.4.2.6 Average latency

Table 9: Latency Time

Rotational speed (RPM)	Time for one revolution (ms)	Average latency (ms)
7200 RPM	8.3	4.17

4.4.3 Drive ready time

Table 10: Drive ready time

Power on to ready	Typical (sec)	Maximum (sec)
80 GB models	6	31
160 GB models	8	31
250 GB models	10	31

Ready The condition in which the drive is able to perform a media access command (for example- read, write) immediately.

Power on This includes the time required for the internal self diagnostics.

Note: Max Power On to ready time is the maximum time period that Device 0 waits for Device 1 to assert PDIAG.

4.4.4 Data transfer speed

Table 11: Data transfer speed

Data transfer speed	250GB model (Mbytes/s)
Disk-Buffer transfer (Zone 0)	
Instantaneous - typical	72.1
Sustained - read typical	61.4
Disk-Buffer transfer (Zone 29)	
Instantaneous - typical	34.9
Sustained - read typical	29.7
Buffer - host (max)	150

- Instantaneous disk-buffer transfer rate (Mbyte/s) is derived by the following formula:

  ```
  512 (Number of sectors on a track) (revolutions per second)
  ```

  Note: The number of sectors per track will vary because of the linear density recording.

- Sustained disk-buffer transfer rate (Mbyte/s) is defined by considering head/cylinder change time for read operation. This gives a local average data transfer rate. It is derived by the following formula:

  ```
  (Sustained Transfer Rate) = A/(B+C+D)
  ```

  where

  ```
  A = 512 (number of data sectors per cylinder)
  B = (number of Surfaces per cylinder – 1) (head switch time)
  C = cylinder change time
  D = (number of surfaces) (time for one revolution)
  ```

- Instantaneous buffer-host transfer rate (Mbyte/s) defines the maximum data transfer rate on the AT Bus. It also depends on the speed of the host.

The method of measurement is given in 4.4.5, “Throughput” on page 19.

4.4.5 Throughput

4.4.5.1 Simple sequential access

The following table illustrates simple sequential access for the three-disk enclosure.

Table 12: Simple Sequential Access performance

Operation	Typical (sec)	Max (sec)
Sequential Read (Zone 0)	0.3	0.32
Sequential Read (Zone 29)	0.61	0.64

The above table gives the time required to read a total of 8000h consecutive blocks (16,777,216 bytes) accessed by 128 read commands. Typical and Max values are given by 105% and 110% of T respectively throughout following performance description.

```
T = A + B + C + 16,777,216/D + 512/E  (READ)
```

where

```
T = Calculated time (sec)
A = Command process time (Command overhead) (sec)
B = Average seek time (sec)
C = Average latency (sec)
D = Sustained disk-buffer transfer rate (byte/sec)
E = Buffer-host transfer rate (byte/sec)
```

Note: It is assumed that a host system responds instantaneously and host data transfer is faster than sustained data rate.

4.4.5.2 Random access

The following table illustrates simple sequential access for three-disk enclosure.

Table 13: Random Access Performance

Operation	Typical (sec)	Max (sec)
Random Read	55.5	58.1

The above table gives the time required to execute a total of 1000h read commands which access a single random LBA. Typical and Max values are given by 105% and 110% of T respectively throughout following performance description.

```
T = 4096(A + B + C+ 512/D + 512/E)  (READ)
```

where

```
T = Calculated time (sec)
A = Command process time (Command overhead) (sec)
B = Average seek time (sec)
C = Latency
D = Average sustained disk-buffer transfer rate (byte/s)
E = Buffer-host transfer rate (byte/s)
```

4.4.6 Operating modes

4.4.6.1 Description of operating modes

Table 14: Description of operating modes

Operating mode	Description
Spin-up	Start up time period from spindle stop or power down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Unload Idle	Spindle rotation at 7200 RPM with heads unloaded.
Idle	Spindle motor and servo system are working normally. Commands can be received and processed immediately.
Standby	Actuator is unloaded and spindle motor is stopped. Commands can be received immediately.
Sleep	TActuator is unloaded and spindle motor is stopped. Only soft reset or hard reset can change the mode to standby.

Note: Upon power down or spindle stop a head locking mechanism will secure the heads in the OD parking position.

4.4.6.2 Mode transition time

Table 15: Mode transition time

From	To	RPM	Transition time (sec)	
			Typical	**Maximum**
Standby	Idle	0 ---> 7200 (3disks)	9	31
Idle	Standby	7200 ---> 0	Immediately	Immediately
Standby	Sleep	0	Immediately	Immediately
Sleep	Standby	0	Immediately	Immediately
Unload idle	Idle	7200	0.7	
Idle	Unload idle	7200	0.7	

"Immediately" means within 1ms.

Note: The command is processed immediately but there will be an actual spin down time reflecting the seconds passed until the spindle motor stops.

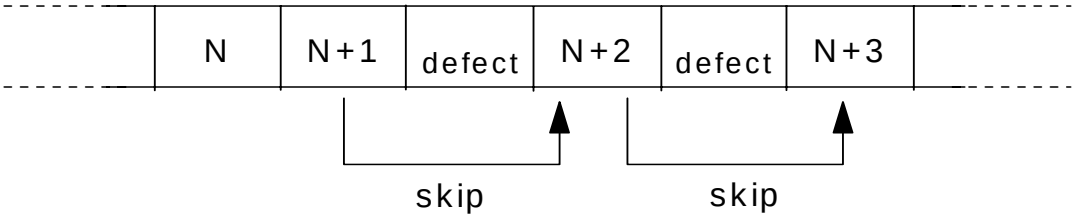
5.0 Defect flagging strategy

Media defects are remapped to the next available sector during the Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internally maintained table.

Shipped format

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by the spare tracks of the inner zone.

Table 16: Plist physical format



Defects are skipped without any constraint, such as track or cylinder boundary.

6.0 Specification

6.1 Jumper settings

6.1.1 Jumper pin location

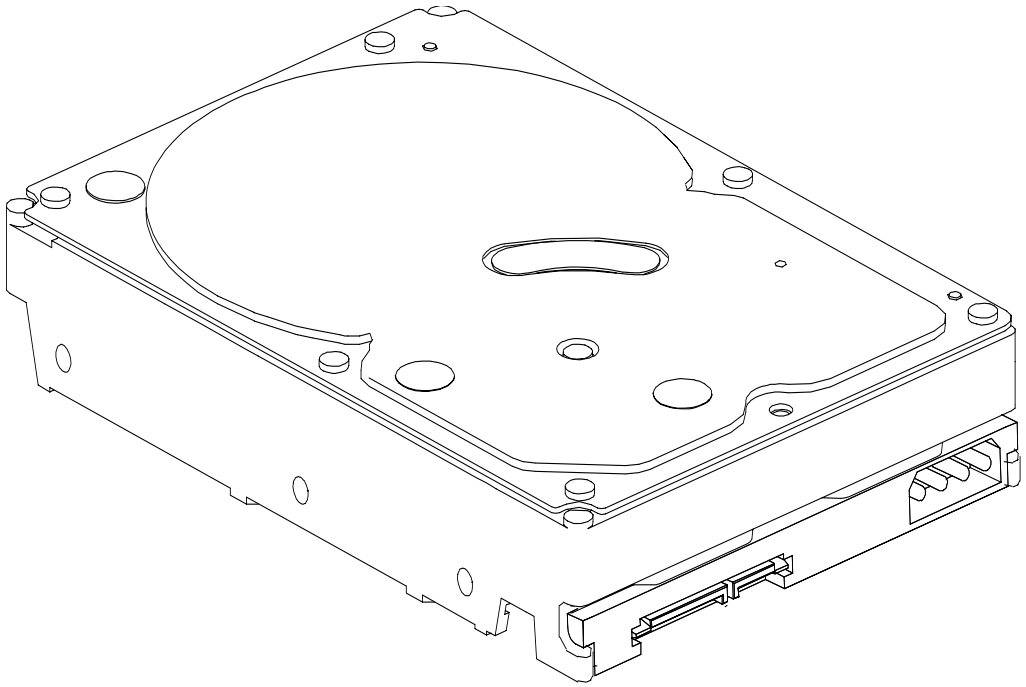
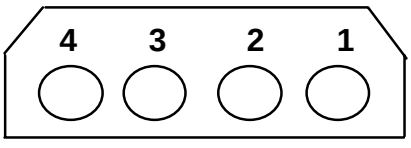


Figure 1: Connector location

6.1.2 4 Pin DC power connector

The DC power connector is designed to mate with AMP part number 1-480424 using AMP pins part number 350078-4 (strip), part number 61173-4 (loose piece), or their equivalents. Pin assignments are shown in the figure below.



Pin	Voltage
1	+12 V
2	GND
3	GND
4	+5V

Figure 2: Power connector pin assignments

6.1.3 Interface Signal Assignments and Descriptions

6.1.3.1 SATA Signal Connector

- The SATA signal connector is a 8-pin connector. Power connector is a 15- pin connector.

6.1.3.2 Signal Definition

- SATA has receivers and drivers to be connected to Tx+/- and Rx +/-. Serial data signal defines the signal names of I/O connector pin and signal name.

Table 17: Interface connector pins and I/O signals

	No.	Plug Connector pin definition		Signal	I/O
Signal	S1	GND	2nd mate	Gnd	
	S2	A+	Differential signal A from Phy	RX+	Input
	S3	A-		RX-	Input
	S4	Gnd	2nd mate	Gnd	
	S5	B-	Differential signal B from Phy	TX-	Output
	S6	B+		TX+	Output
	S7	Gnd	2nd mate	Gnd	
Key and spacing separate signal and power segments					
	P1	V33	3.3V power	3.3V	
Power	P2	V33	3.3V power	3.3V	
	P3	V33	3.3V power, pre-charge, 2nd Mate	3.3V	
	P4	Gnd	1st mate	Gnd	
	P5	Gnd	2nd mate	Gnd	
	P6	Gnd	2nd mate	Gnd	
	P7	V5	5V power,pre-charge,2nd Mate	5V	
	P8	V5	5V power	5V	
	P9	V5	5V power	5V	
	P10	Gnd	2nd mate	Gnd	
	P11	Reserved	1. This pin corresponding to P11 in theback-plane receptacle connector is also reserved. 2. The corresponding pin to be mated with P11 in the power cable receptacle connector shall always be grounded.	Reserve	
	P12	Gnd	1st mate	Gnd	
	P13	V12	12V power,pre-chage,2nd mate	V12	
	P14	V12	12V power	V12	
	P15	V12	12V power	V12	

6.1.3.3 TX+ / TX-

These signal are the outbound high-speed differrential signals that are connected to the serial ATA cable.

6.1.3.4 RX+ / RX

These signals are the inbound high-speed differential signals that are connected to the serial ATA cable.

The following standard shall be referenced about signal specifications.

Serial ATA: High Speed Serialized AT Attachment Revision 1.0a 7-January - 2003

6.1.3.5 Out of band signaling

Figure XX shows the timing of COMRESET, COMINIT and COMWAKE.

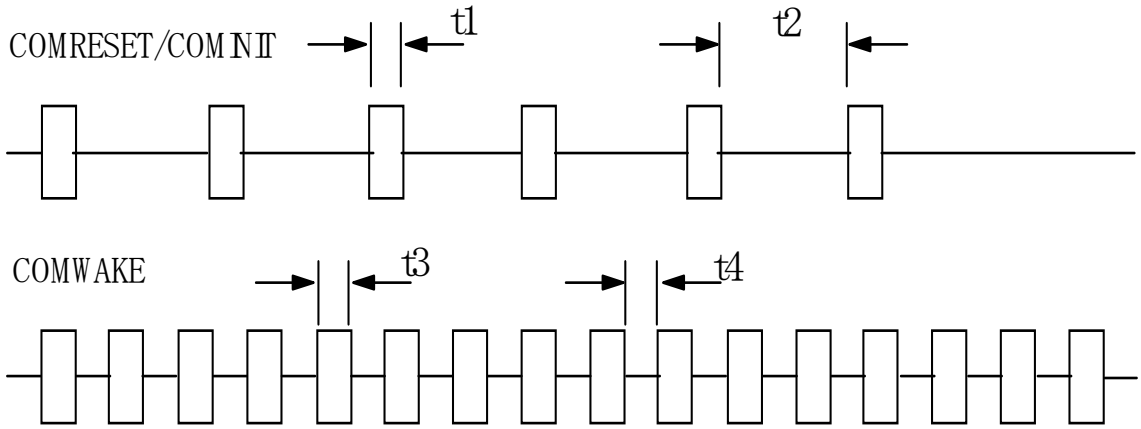


Figure 3: Timing of COMRESET, COMINIT and COMWAKE

Table 18: Parameter Description

	PARAMETER DESCRIPTION	Nominal (ns)
t1	ALINE primitives	106.7
t2	Spacing	320
t3	ALIGN primitives	106.7
t4	Psacing	106.7

6.2 Environment

6.2.1 Temperature and humidity

Table 19: Temperature and humidity

Operating conditions	
Temperature	5C to 55ºC (See note below)
Relative humidity	8 to 90%, non-condensing
Maximum wet bulb temperature	29.4ºC, non-condensing
Maximum temperature gradient	15ºC/hour
Altitude	–300 to 3,048 m
Non-operating conditions	
Temperature	–40C to 65ºC
Relative humidity	5 to 95%, non-condensing
Maximum wet bulb temperature	35ºC, non-condensing
Altitude	–300 to 12,000 m

Notes:

•The system is responsible for providing sufficient ventilation to maintain a surface temperature below 60°C at the center of the top cover of the drive.

•Noncondensing conditions should be maintained at any time.

•Maximum storage period within shipping package is one year.

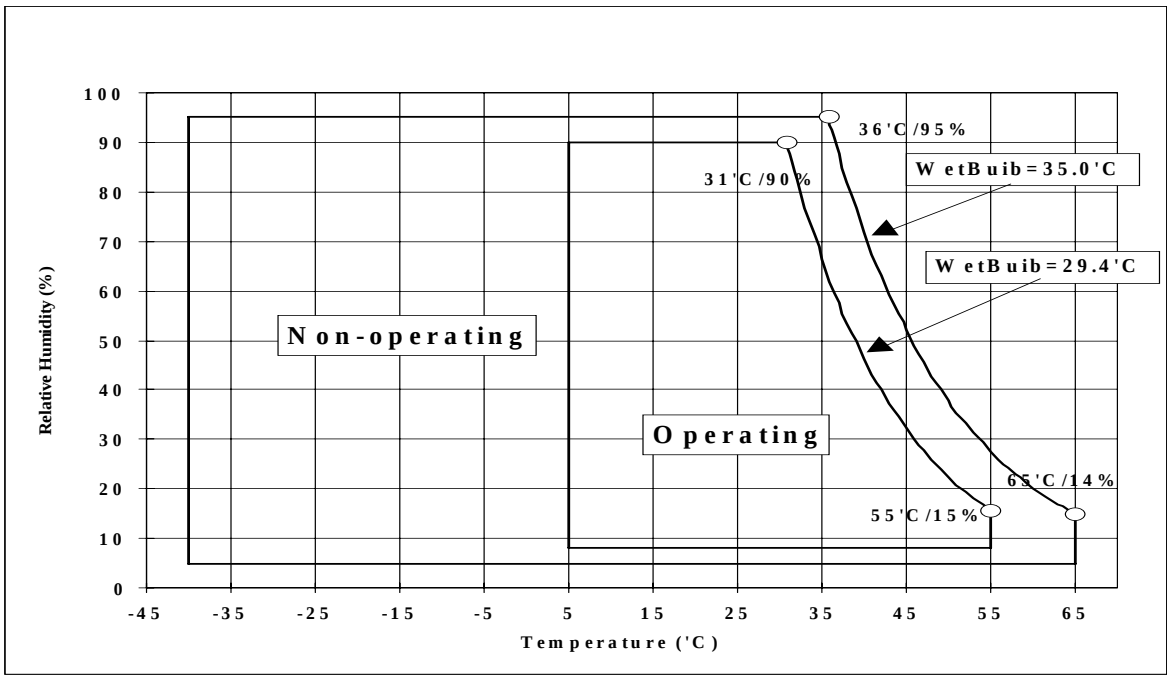


Figure 4: Limits of temperature and humidity

6.2.2 Corrosion test

The drive shows no sign of corrosion inside and outside of the hard disk assembly and is functional after being subjected to seven days at 50°C with 90% relative humidity.

6.3 DC power requirements

Damage to the drive electronics may result if the power supple cable is connected or disconnected to the legacy power connector while power is being applied to the drive (no hot plug/unplug is alloweed). If SATA power supply cable is connected or disconnected to the SATA power connector, hot plug/unplug is allowed.

6.3.1 Input voltage

Table 20: Input voltage

Input voltage supply[2]	During run and spin up	Absolute max spike voltage[1]
+5 V	5 V ± 5%	–0.3 to 7 V
+12 V	12 V + 10% –8%	–0.3 to 15 V

[1] *To avoid damage to the drive electronics, power supply voltage spikes must not exceed specifications.*

[2] *+12V should be applied within 60 seconds after +5V is applied to the drive.*

6.3.2 Power supply current (typical)

Table 21: Power supply current of models

Power supply current of 250-GB model values in milliamps, RMS	+5 Volts (mA)		+12 Volts (mA)		Total (W)
	Pop mean	Std dev	Pop mean	Std dev	
Idle average	400	12	470	12	7.6
Idle ripple (peak-to-peak)	230	40	320	20	
Low RPM idle	230	7	180	10	3.3
Low RPM idle ripple	220	25	270	20	
Unload idle average	230	7	350	13	5.4
Unload idle ripple	220	25	240	20	
Random R/W average	540	9	660	14	10.6
Random R/W peak	1342	30	1750	50	
Silent R/W average[2]	570	9	470	15	8.5
Silent R/W peak	1342	30	890	40	
Start up (max)	960	50	1840	75	
Standby average	230	9	20	3	1.4
Sleep average	190	8	20	3	1.2

Except for a peak of less than 100 ms duration

[1] Random seeks at 40% duty cycle

[2] Seek duty = 30%, W/R duty = 45%, Idle duty = 25%

Power supply current of 120 GB and 160 GB models values in milliamps, RMS	**+5 Volts (mA)**		**+12 Volts (mA)**		**Total (W)**
	Pop mean	Std dev	Pop mean	Std dev	
Idle average	400	12	375	12	6.5
Idle ripple (peak-to-peak)	230	40	250	20	
Low RPM idle	230	7	140	10	2.8
Low RPM idle ripple	220	25	170	20	
Unload idle average	230	7	300	13	4.8
Unload idle ripple	220	25	200	20	
Random R/W average	520	9	590	12	9.8
Random R/W peak	1342	30	1600	50	
Silent R/W average[2]	570	9	390	12	7.5
Silent R/W peak	1342	50	890	40	
Start up (max)	960	50	1750	50	
Standby average	230	9	20	3	1.4
Sleep average	190	8	20	3	1.2

Power supply current of 40GB and 80GB models values in milliamps, RMS	**+5 Volts (mA)**		**+12 Volts (mA)**		**Total (W)**
	Pop mean	Std dev	Pop mean	Std dev	
Idle average	400	12	300	12	5.6
Idle ripple (peak-to-peak)	230	40	220	20	
Low RPM idle	230	7	130	10	2.7
Low RPM idle ripple	220	25	160	20	
Unload idle average	230	7	270	12	4.4
Unload idle ripple	220	25	200	20	
Random R/W average	540	9	590	12	9.8
Random R/W peak	1342	50	1720	65	
Silent R/W average[2]	570	9	370	12	7.3
Silent R/W peak	1342	50	830	40	

Power supply current of 40GB and 80GB models values in milliamps, RMS	**+5 Volts (mA)**		**+12 Volts (mA)**		**Total (W)**
	Pop mean	Std dev	Pop mean	Std dev	
Start up (max)	960	50	1700	50	
Standby average	230	9	20	3	1.4
Sleep average	190	8	20	3	1.2

1 Random R/W, Silent R/W : 40 IOPS / 16 Blocks Random Write and Random Read.

6.3.3 Power supply generated ripple at drive power connector

Table 22: Power supply generated ripple at drive power connector

	Maximum (mV pp)	MHz
+5 V dc	100	0-10
+12 V dc	150	0-10

During drive start up and seeking 12-volt ripple is generated by the drive (referred to as dynamic loading). If the power of several drives is daisy chained together, the power supply ripple plus the dynamic loading of the other drives must remain within the above regulation tolerance. A common supply with separate power leads to each drive is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the performance of the drive, the drive must be held by four screws in a user system frame which has no electrical level difference at the four screws position and has less than ±300 millivolts peak to peak level difference to the ground of the drive power connector.

6.4 Reliability

6.4.1 Data integrity

No more than one sector is lost at Power loss condition during the write operation when the write cache option is disabled. If the write cache option is active, the data in write cache will be lost. To prevent the loss of customer data, it is recommended that the last write access before power off be issued after setting the write cache off.

6.4.2 Cable noise interference

To avoid any degradation of performance throughput or error rate when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

6.4.3 Start/stop cycles

The drive withstands a minimum of 50,000 start/stop cycles in a 40° C environment and a minimum of 10,000 start/stop cycles in extreme temperature or humidity within the operating range. See Table 19: “Temperature and humidity” on page 26 and Figure 4: “Limits of temperature and humidity” on page 26.

6.4.4 Preventive maintenance

None

6.4.5 Data reliability

Probability of not recovering data is 1 in 10^{14} bits read

ECC On The Fly correction

- 1 Symbol : 8 bits
- 4 Interleave
- 12 ECCs are embedded into each interleave
- This implementation always recovers 5 random burst errors and a 153-bit continuous burst error

6.4.6 Required power-off sequence

The required BIOS sequence for removing power from the drive is as follows:

Step 1: Issue one of the following commands.

Standby
Standby immediate
Sleep

Note: Do not use the Flush Cache command for the power off sequence because this command does not invoke Unload

Step 2: Wait until the Command Complete status is returned. In a typical case 350 ms are required for the command to finish completion; however, the BIOS time out value needs to be 30 seconds considering error recovery time. Refer to section12.0 “Timings” on page 67.

Step 3: Terminate power to HDD.

6.5 Mechanical specifications

6.5.1 Physical dimensions and weight

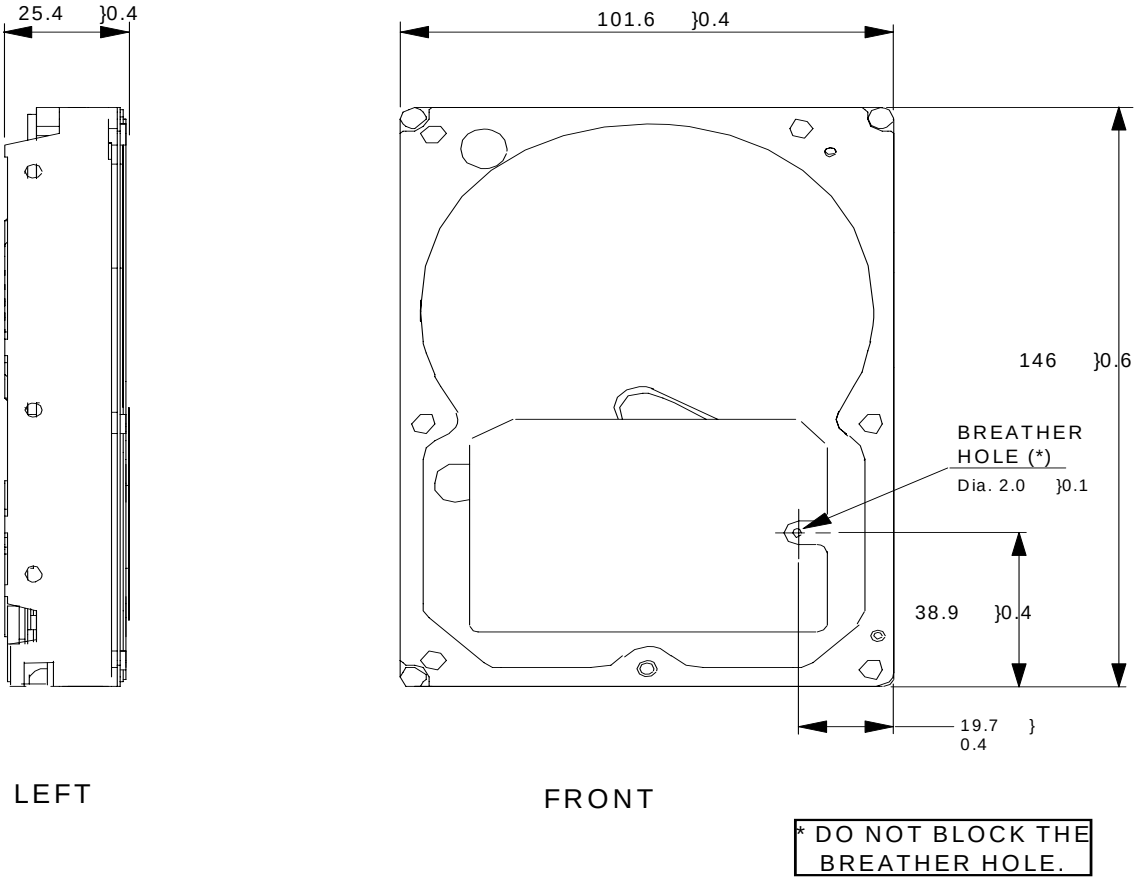


Figure 5: Top and side view of 120GB - 250GB models with mechanical dimensions

All dimensions in the above figure are in millimeters.

The breather hole must be kept uncovered in order to keep the air pressure inside of the disk enclosure equal to external air pressure.

The following table lists the dimensions of the drive.

Table 23: Physical dimensions and weight

Height [mm]	25.4±0.4
Width [mm]	101.6±0.4
Length [mm]	146.0±0.6
Weight [grams - maximum]	640

6.5.2 Mounting hole locations

The mounting hole locations and size of the drive are shown below. All dimensions are in mm.

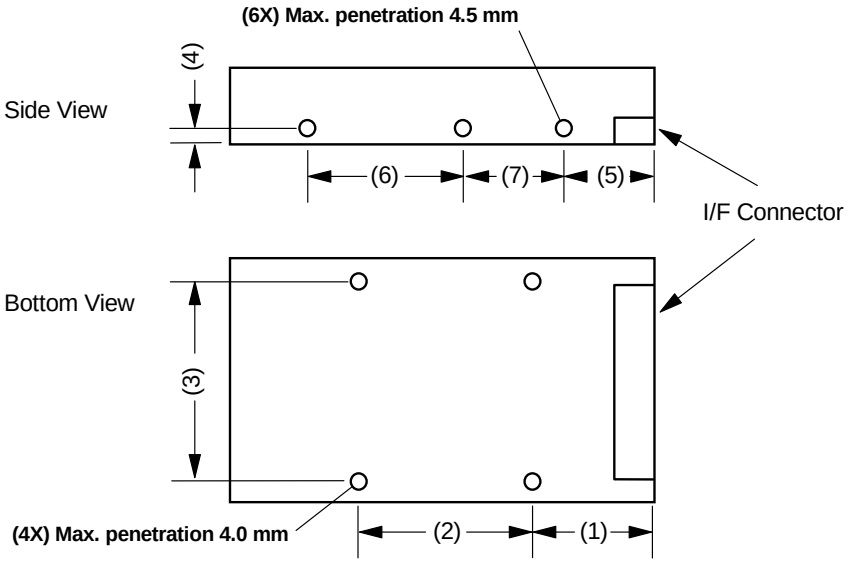


Figure 6: Mounting hole locations

Thread	(1)	(2)	(3)	(4)	(5)	(6)	(7)
6-32 UNC	41.28±0.5	44.45±0.2	95.25±0.2	6.35±0.2	28.5±0.5	60.0±0.2	41.6±0.2

6.5.3 Connector locations

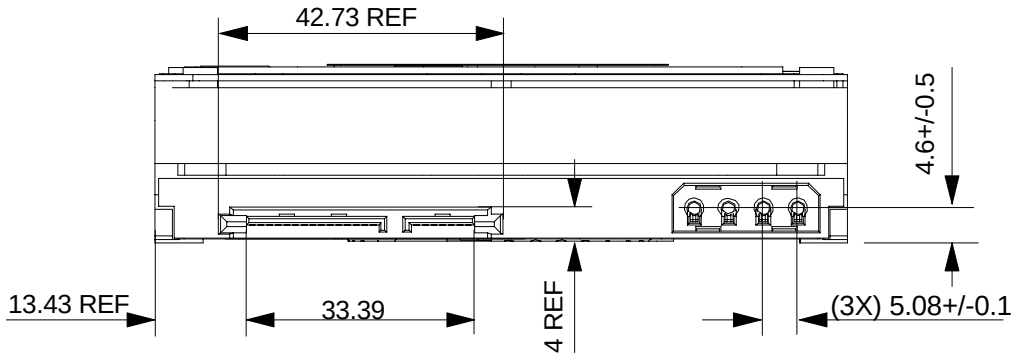


Figure 7: Connector locations

6.5.4 Drive mounting

The drive will operate in all axes (6 directions). Performance and error rate will stay within specification limits if the drive is operated in the other orientations from which it was formatted.

For reliable operation, the drive must be mounted in the system securely enough to prevent excessive motion or vibration of the drive during seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

The recommended mounting screw torque is 0.6 - 1.0 Nm (6-10 Kgf.cm).

The recommended mounting screw depth is 4 mm maximum for bottom and 4.5 mm maximum for horizontal mounting.

Drive level vibration test and shock test are to be conducted with the drive mounted to the table using the bottom four screws.

6.5.5 Heads unload and actuator lock

The head load/unload mechanism is provided to protect the disk data during shipping, movement, or storage. Upon power down, the heads are automatically unload from the disk area and the locking mechanism of the head actuator will secure the heads in unload position.

6.6 Vibration and shock

All vibration and shock measurements recorded in this section are made with a drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

6.6.1 Operating vibration

6.6.1.1 Random vibration

The test is 30 minutes of random vibration using the power spectral density (PSD) levels shown below in each of three mutually perpendicular axes. The disk drive will operate without non-recoverable errors when subjected to the above random vibration levels.

The overall RMS (root mean square) level is 0.67 G for horizontal vibration and 0.56 G for vertical.

Table 24: Random vibration PSD

Table 25: Random vibration PSD profile break points (operating)

Direction	5Hz	17Hz	45Hz	48Hz	62Hz	65Hz	150Hz	200Hz	500Hz	RMS (G)
Horizontal x10–3 [G2/Hz	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5	0.67
Vertical x10–3 [G2/Hz]	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.08	0.08	0.56

The overall RMS (root mean square) level is 0.67 G for horizontal vibration and 0.56 G for vertical.

6.6.1.2 Swept sine vibration

The drive will meet the criteria shown below while operating in the specified conditions:

- No errors occur with 0.5 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3-minute dwells at two major resonances
- No data loss occurs with 1 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3-minute dwells at two major resonances

6.6.2 Nonoperating vibration

The drive does not sustain permanent damage or loss of previously recorded data after being subjected to the environment described below

6.6.2.1 Random vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes for a duration of 10 minutes per axis. The PSD levels for the test simulate the shipping and relocation environment shown below.

Table 26: Random Vibration PSD profile breakpoints (nonoperating)

Frequency	2Hz	4Hz	8Hz	40Hz	55Hz	70Hz	200Hz
G2/Hz	0.001	0.03	0.03	0.003	0.01	0.01	0.001

The overall RMS (root mean square) level of vibration is 1.04 G.

6.6.2.2 Swept sine vibration

- 2 G (zero-to-peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

6.6.3 Operating shock

The drive meets the following criteria while operating in the conditions described below. The shock test consists of 10 shock inputs in each axis and direction for total of 60. There must be a delay between shock pulses long enough to allow the drive to complete all necessary error recovery procedures.

- No error occurs with a 10 G half-sine shock pulse of 11 ms duration in all models.
- No data loss occurs with a 30 G half-sine shock pulse of 4 ms duration in all models.
- No data loss occurs with a 55 G half-sine shock pulse of 2 ms duration in all models.

6.6.4 Nonoperating shock

The drive will operate with no degradation of performance after being subjected to shock pulses with the following characteristics.Trapezoidal shock wave

6.6.4.1 Trapezoidal shock wave

- Approximate square (trapezoidal) pulse shape
- Approximate rise and fall time of pulse is 1 ms
- Average acceleration level is 50 G. (Average response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time "duration of 11 ms")
- Minimum velocity change is 4.23 meters per second

6.6.4.2 Sinusoidal shock wave

The shape is approximately half-sine pulse. The figure below shows the maximum acceleration level and duration.

Table 27: Sinusoidal shock wave

Models	Acceleration level (G)	Duration (ms)
1 and 2 disk models	350	2
3 disk models	300	
All models	75	11

6.6.5 Nonoperating rotational shock

All shock inputs shall be applied around the actuator pivot axis.

Table 28: Rotational shock

Duration	Rad/s^2
1 ms	30,000
2 ms	20,000

6.7 Acoustics

The upper limit criteria of the octave sound power levels are given in Bels relative to one picowatt and are shown in the following table. The sound power emission levels are measured in accordance with ISO7779.

Table 29: Sound power levels

Mode		Typical/Max		
		1 disk model	2 disk model	3 disk model
Idle		2.6 / 3.0	2.8 / 3.2	3.0 / 3.4
Operating	Performance seek mode	3.4 / 3.7	3.4 / 3.7	3.4 / 3.7
	Quiet seek	2.8 / 3.2	2.9 / 3.3	3.1 / 3.5

Table 30: Sound power levels

Mode definitions

- I**dle mode:** The drive is powered on, disks spinning, track following, unit is ready to receive and respond to control line commands.
- **Operating mode:** Continuous random cylinder selection and seek operation of the actuator with a dwell time at each cylinder. The seek rate for the drive is calculated with the following formula:
  - Dwell time = 0.5 x 60/RPM
  - Seek rate = 0.4 / (average seek time + dwell time)

6.8 Identification labels

The following labels are affixed to every drive:

- A label containing the Hitachi logo, the Hitachi Global Storage Technologies part number and the statement " Made by Hitachi Global Storage Technologies Inc." or Hitachi Global Storage Technologies approved equivalent.
- A label containing the drive model number, the manufacturing date code, the formatted capacity, the place of manufacture, UL/CSA/TUV/CE/C-Tick mark logos
- A bar code label containing the drive serial number
- A label containing jumper pin description
- A user designed label per agreement

The above labels may be integrated with other labels

6.9 Safety

6.9.1 UL and CSA approval

The product is qualified per UL (Underwriters Laboratory) 1950 Third Edition and CAN/CSA C22.2 No.950-M95 Third Edition, for use in Information Technology Equipment, including Electric Business Equipment. The UL Recognition or the CSA certification is maintained for the product life. The UL and C-UL recognition mark or the CSA monogram for CSA certification appears on the drive.

6.9.2 German safety mark

All models are approved by TUV on Test Requirement: EN60950:1992+A1-4, but the GS mark is not applicable to internal devices such as this product.

6.9.3 Flammability

The printed circuit boards used in this drive are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better. However, small mechanical parts such as cable ties, washers, screws, and PC board mounts may be made of material with a UL recognized flammability rating of V-2.

6.9.4 Safe handling

The product is conditioned for safe handling in regards to sharp edges and corners.

6.9.5 Environment

The product does not contain any known or suspected carcinogens.

Environmental controls meet or exceed all applicable government regulations in the country of origin. Safe chemical usage and manufacturing control are used to protect the environment. An environmental impact assessment has been done on the manufacturing process used to build the drive, the drive itself and the disposal of the drive at the end of its life.

Production also meets the requirements of the international treaty on chlorofluorocarbon (CFC) control known as the United Nations Environment Program Montreal Protocol, and as ratified by the member nations. Material to be controlled include CFC-11, CFC-12, CFC-113, CFC-114, CFC-115, Halon 1211, Halon 1301 and Halon 2402. Although not specified by the Protocol, CFC-112 is also controlled. In addition to the Protocol Hitachi Global Storage Technologies requires the following:

- that no packaging used for the shipment of the product use controlled CFCs in the manufacturing process.
- that no manufacturing processes for parts or assemblies include printed circuit boards use controlled CFC materials.

6.9.6 Secondary circuit protection

Spindle/VCM driver module includes 12 V over current protection circuit

6.10 Electromagnetic compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate meets the worldwide EMC requirements listed below:

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15. (A 6 dB buffer shall be maintained on the emission requirements).

•European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP). IBM National Bulletin NB 2-0001-400, NB 2-0001-401, and NB 2-0001-403.

6.10.1 CE mark

The product is declared to be in conformity with requirements of the following EC directives under the sole responsibility of Hitachi Global Storage Technologies Japan Ltd:

Council Directive 89/336/EEC on the approximation of laws of the Member States relating to electromagnetic compatibility.

6.10.2 C-TICK mark

The product complies with the following Australian EMC standard:

Limits and methods of measurement of radio disturbance characteristics of information technology, AS/NZS 3548 :1995 Class B.

6.10.3 BSMI mark

The product complies with the Taiwan EMC standard"Limits and methods of measurement of radio disturbance characteristics of information technology equipment, CNS 13438 Class B."

6.11 Packaging

Drives are packed in ESD protective bags and shipped in appropriate containers.

7.0 General

7.1 Introduction

This specification describes the host interface of the HDS7225xxVLSAx0 hard disk drive.

The interface conforms to the Working Document of Information technology - Serial ATA: High Speed Serialized AT Attachment Revision 1.0a dated on 7 January 2003 with certain limitations described in 8.2, "Deviations From Standard."

Device	Device indicates HDS7225xxVLSAx0
Host	Host indicates the system that the device is attached to.

7.2 Deviations from standard

The device conforms to the referenced specifications with the following deviations:

COMReset COMReset resposne is not the same as that of power on reset. Refer to section 5.1 "Reset Response" for detail.

Device/Head Register Device/Head Register bit 5 and 7 are 1

8.0 Registers

In Serial ATA, the host adapter contains a set of registers that shadow the contents of the traditional device registers, referred to as the Shadow Register Block. Shadow Register Block registers are interface registers used for delivering commands to the device or posting status from the device. About details, please refer to the Serial ATA Spec.

In the following cases, the host adapter sets the BSY bit in its shadow Status Register and then transmits a fram to the device containing the new regster contents.

- Command register is written in the Shadow Register Block

- Device Control register is written in the Shadow Register Block with a change of state of the SRST bit

- COMRESET is requested

8.1 Device/Head Register

Table 31: Device Head/Register

7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

This register contains the device and head numbers.

Bit	Definitions
L	Binary encoded address mode select. When L = 0, addressing is by CHS mode. When L = 1, addressing is by LBA mode.
DRV	Device. When DRV=0, device 0 (master) is selected. This bit is reserved since all Serial ATA devices behave like Device 0 devices.
HS3, HS2, HS1, HS0	Head Select. These four bits indicate the binary encoded address of the head. Bit HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head. The head number may be from zero to the number of heads minus one. In LBA mode, HS3 through HS0 contain bits 24–27 of the LBA. At command completion these bits are updated to reflect the current LBA bits 24–27.

9.0 General operation

9.1 Reset response

ATA has the following three types of resets:

Power On Reset (POR) — The device executes a series of electrical circuitry diagnostics, spins up the head disk assembly, tests speed and other mechanical parametric, and sets default values.

COMRESET — COMRESET- signal is negated in Serial ATA Bus.

The device resets the interface circutitry as well as Soft Reset.

Soft Reset (Software Reset) — The SRST bit in the Device Control Register is set and then is reset. The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset are shown in the table below.

Table 32: Reset response table

	POR	hard reset	soft reset
Aborting Host interface	-	O	O
Aborting Device operation	-	(*1)	(*1)
Initialization of hardware	O	X	X
Internal diagnostic	O	X	X
Spinning spindle	O	X	X
Initialization of registers (*2)	O	O	O
Reverting programmed parameters to default Number of CHS (set by Initialize Device Parameters) Multiple mode Write Cache Read look-ahead ECC bytes	O	(*3)	(*3)
Disable Standby timer	0	x	x
Power mode	(*5)	(*4)	(*4)

O – execute X – does not execute

Notes:

(*1) Execute after the data in write cache has been written.

(*2) The default value on POR is shown in Table 33: “Default Register Values” on page 46.

(*3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

(*4) In the case of Sleep mode, the device goes to Standby mode. In other cases, the device does not change current mode.

(*5) Idle when Power-Up in Standby feature set is disabled. Standby when Power-Up in Standby feature set is enabled.

9.2 Register initialization

After a power on, a hard reset, or a software reset, the register values are initialized as shown in the table below.

Table 33: Default Register Values

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	A0h
Status	50h
Alternate Status	50h

After power on, COMRESET, software reset, the register values are initialized as shown in Figure 3.

Table 34: Diagnostic codes

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Device Diagnostic command is shown in Table 38.

9.3 Diagnostic and Reset considerations

In each case of Power on Reset, COMRESET, Soft reset, and the EXECUTE DEVICE DIAGNOSTIC command, the device is diagnosed. And the Error register is set as shown in Figure 3 ,4.

9.4 Power Management Mode (Slumber and Partial)

Power Management Mode is not supported. Device ignores the signals of PMREQ_S/PMREQ_P from Host. Please refer to the Serial ATA Specification about Power Management Mode.

10.0 Command protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

Please refer to Serial ATA Revision 1.0a (Sector 9. device command layer protocol) about each protocols.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a COMRESET or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

10.1 PIO Data In commands

The following are Data In commands:

- Device Configuration Identity
- Identify Device
- Read Buffer
- Read Log Ext
- Read Long
- Read Multiple
- Read Multiple Ext
- Read Sector(s)
- Read Sector(s) Ext
- S.M.A.R.T. Read Attribute Values
- S.M.A.R.T. Read Attribute Thresholds
- S.M.A.R.T. Read log sector

Execution includes the transfer of one or more 512 byte (> 512 bytes on Read Long) sectors of data from the device to the host.

10.2 PIO Data Out Commands

The following are Data Out commands:

- Device Configuration SET
- Format Track
- Security Disable Password
- Security Erase Unit

- Security Set Password
- Security Unlock
- Set Max Set Password
- Set Max Unlock
- S.M.A.R.T. Write log sector
- Write Buffer
- Write Log Ext
- Write Long
- Write Multiple
- Write Multiple Ext
- Write Sector(s)
- Write Sector(s) Ext

Execution includes the transfer of one or more 512 byte (> 512 bytes on Write Long) sectors of data from the host to the device.

10.3 Non-data commands

The following are Non-data commands:

- Check Power Mode
- Device Configuration FREEZE LOCK
- Device Configuration RESTORE
- Execute Device Diagnostic
- Flush Cache
- Flush Cache Ext
- Idle
- Idle Immediate
- Initialize Device Parameters
- NOP
- Read Native Max ADDRESS
- Read Native Max ADDRESS Ext
- Read Verify Sector(s)
- Read Verify Sector(s) Ext
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Max ADDRESS
- Set Max ADDRESS Ext
- Set Max LOCK
- Set Max FREEZE LOCK
- Set Multiple Mode
- Sleep
- S.M.A.R.T. Disable Operations
- S.M.A.R.T. Enable/Disable Attribute Autosave

- S.M.A.R.T. Enable/Disable Automatic Off Line
- S.M.A.R.T. Enable Operations
- S.M.A.R.T. Execute Off-line Data Collection
- S.M.A.R.T. Return Status
- S.M.A.R.T. Save Attribute Values
- Standby
- Standby Immediate

Execution of these commands involves no data transfer:

10.4 DMA data in commands

The following are DMA commands:

- Read DMA
- Read DMA Ext

Execution of this class of commadn included the transfer of one or more blocks of data from the devince to the host using DMA transfer.

10.5 DMA data out Commands

These commands are:

Write DMA

Write DMA Ext

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device using DMA transfer. A single interrupt is issued at the completion of the successful transfer of all data required by the command.

10.6 DMA queued commands

These commands are:

- Read DMA Queued
- Read DMA Queued Ext

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host using DMA transfer. All data for the command may be transferred without a bus release between the command receipt and the data transfer. This command may bus release before transferring data. The host shall initialize the DMA controller prior to transferring data. When data transfer is begun, all data for the request shall be transferred without a bus release.

10.6.1 Write DMA Queued Commands

These commands are:

- Write DMA Queued
- Write DMA Queued Ext

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host using DMA transfer. All data for the command may be transferred without a bus release between the command receipt and the data transfer. This command may bus release before transferring data. The host shall initialize the

DMA controller prior to transferring data. When data transfer is begun, all data for the request shall be transferred without a bus release.

10.6.2 Service Commands

This command is:

- Service

11.0 Command descriptions

The table below shows the commands that are supported by the device. Table 37: “Command Set (subcommand)” on page 53 shows the subcommands that are supported by each command or feature.

Table 35: Command Set (1 of 2)

Protocol	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0
3	Check Power Mode	E5	1 1 1 0 0 1 0 1
3	Check Power Mode*	98	1 0 0 1 1 0 0 0
3	Device Configuration RESTORE	B1	1 0 1 1 0 0 0 1
3	Device Configuration FREEZE LOCK	B1	1 0 1 1 0 0 0 1
1	Device Configuration IDENTIFY	B1	1 0 1 1 0 0 0 1
2	Device Configuration SET	B1	1 0 1 1 0 0 0 1
3	Execute Device Diagnostic	90	1 0 0 1 0 0 0 0
3	Flush Cache	E7	1 1 1 0 0 1 1 1
3	Flush Cache Ext	EA	1 1 1 0 1 0 1 0
2	Format Track	50	0 1 0 1 0 0 0 0
3	Format Unit	E7	1 1 1 1 0 1 1 1
1	Identify Device	EC	1 1 1 0 1 1 0 0
3	Idle	E3	1 1 1 0 0 0 1 1
3	Idle*	97	1 0 0 1 0 1 1 1
3	Idle Immediate	E1	1 1 1 0 0 0 0 1
3	Idle Immediate*	95	1 0 0 1 0 1 0 1
3	Initialize Device Parameters	91	1 0 0 1 0 0 0 1
3	NOP	00	0 0 0 0 0 0 0 0
1	Read Buffer	E4	1 1 1 0 0 1 0 0
4	Read DMA	C8	1 1 0 0 1 0 0 0
4	Read DMA	C9	1 1 0 0 1 0 0 1
4	Read DMA Ext	25	0 0 1 0 0 1 0 1
5	Read DMA Queued	C7	1 1 0 0 0 1 1 1
5	Read DMA Queued Ext	26	0 0 1 0 0 1 1 0
1	Read Long	22	0 0 1 0 0 0 1 0
1	Read Long	23	0 0 1 0 0 0 1 1
1	Read Log Ext	2F	0 0 1 0 1 1 1 1
1	Read Multiple	C4	1 1 0 0 0 1 0 0
1	Read Multiple Ext	29	0 0 1 0 1 0 0 1
3	Read Native Max ADDRESS	F8	1 1 1 1 1 0 0 0
3	Read Native Max ADDRESS Ext	27	0 0 1 0 0 1 1 1
1	Read Sector(s)	20	0 0 1 0 0 0 0 0
1	Read Sector(s)	21	0 0 1 0 0 0 0 1
1	Read Sector(s) Ext	24	0 0 1 0 0 1 0 0
3	Read Verify Sector(s)	40	0 1 0 0 0 0 0 0
3	Read Verify Sector(s)	41	0 1 0 0 0 0 0 1
3	Read Verify Sector(s) Ext	42	0 0 0 1 - - - -
3	Recalibrate	1x	0 0 0 1 - - - -
2	Security Disable Password	F6	1 1 1 1 1 0 1 0
3	Security Erase Prepare	F3	1 1 1 1 0 0 1 1
2	Security Erase Unit	F4	1 1 1 1 0 1 0 0

Table 36: Command Set (2 of 2)

Protocol	Command	Code (Hex)	Binary Code Bit							
			7	6	5	4	3	2	1	0
3	Security Freeze Lock	F5	1	1	1	1	0	1	0	1
2	Security Set Password	F1	1	1	1	1	0	0	0	1
2	Security Unlock	F2	1	1	1	1	0	0	1	0
3	Seek	7x	0	1	1	1	-	-	-	-
5	Service	A2	1	0	1	0	0	0	1	0
3	Set Features	EF	1	1	1	0	1	1	1	1
3	Set Max ADDRESS	F9	1	1	1	1	1	0	0	1
3	Set Max ADDRESS Ext	37	0	0	1	1	0	1	1	1
3	Set Multiple Mode	C6	1	1	0	0	0	1	1	0
3	Sleep	E6	1	1	1	0	0	1	1	0
3	Sleep*	99	1	0	0	1	1	0	0	1
3	S.M.A.R.T. Disable Operations	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Enable/Disable Attribute Auto save	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Enable/Disable Automatic Off-line	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Enable Operations	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Execute Off-line Data Collection	B0	1	0	1	1	0	0	0	0
1	S.M.A.R.T. Read Attribute Values	B0	1	0	1	1	0	0	0	0
1	S.M.A.R.T. Read Attribute Thresholds	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Return Status	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Save Attribute Values	B0	1	0	1	1	0	0	0	0
2	S.M.A.R.T. Write Log Sector	B0	1	0	1	1	0	0	0	0
3	Standby	E2	1	1	1	0	0	0	1	0
3	Standby*	96	1	0	0	1	0	1	1	0
3	Standby Immediate	E0	1	1	1	0	0	0	0	0
3	Standby Immediate*	94	1	0	0	1	0	1	0	0
2	Write Buffer	E8	1	1	1	0	1	0	0	0
4	Write DMA	CA	1	1	0	0	1	0	1	0
4	Write DMA	CB	1	1	0	0	1	0	1	1
4	Write DMA Ext	35	0	0	1	1	0	1	0	1
5	Write DMA Queued	CC	1	1	0	0	1	1	0	0
5	Write DMA Queued Ext	36	0	0	1	1	0	1	1	0
2	Write Log Ext	3F	0	0	1	1	1	1	1	1
2	Write Long	32	0	0	1	1	0	0	1	0
2	Write Long	33	0	0	1	1	0	0	1	1
2	Write Multiple	C5	1	1	0	0	0	1	0	1
2	Write Multiple Ext	39	0	0	1	1	1	0	0	1
2	Write Sector(s)	30	0	0	1	1	0	0	0	0
2	Write Sector(s)	31	0	0	1	1	0	0	0	1
2	Write Sector(s)Ext	34	0	0	1	1	0	1	0	0

Commands marked * are alternate command codes for previously defined commands

Protocol: 1 : PIO data IN command

```
2 : PIO data OUT command
3 : Non data command
4 : DMA command
5 :
```

Table 37: Command Set (subcommand)

Command (Subcommand)	Command Code (Hex)	Feature Register (Hex)
S.M.A.R.T. Function		
S.M.A.R.T. Read Attribute Values	B0	D0
S.M.A.R.T. Read Attribute Thresholds	B0	D1
S.M.A.R.T. Enable/Disable Attribute Autosave	B0	D2
S.M.A.R.T. Save Attribute Values	B0	D3
S.M.A.R.T. Execute Off-line Immediate	B0	D4
S.M.A.R.T. Read Log	B0	D5
S.M.A.R.T. Write Log	B0	D6
S.M.A.R.T. Enable Operations	B0	D8
S.M.A.R.T. Disable Operations	B0	D9
S.M.A.R.T. Return Status	B0	DA
S.M.A.R.T. Enable/Disable Automatic Off-line	B0	DB
Set Features		
Enable Write Cache	EF	02
Set Transfer mode	EF	03
Enable Advanced Power Management	EF	05
Enable Power-up in Standby Feature Set	EF	06
Power-up in Standby Feature Set Device Spin-up	EF	07
Enable Address Offset mode	EF	09
Enable Automatic Acoustic Management	EF	42
52 bytes of ECC apply on Read/Write Long	EF	44
Disable read look-ahead feature	EF	55
Enable release interrupt	EF	5D
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Disable Advanced Power Management	EF	85
Disable Power-up in Standby Feature Set	EF	86
Disable Address Offset mode	EF	89
Enable read look-ahead feature	EF	AA
4 bytes of ECC apply on Read/Write Long	EF	BB
Disable Automatic Acoustic Management	EF	C2
Enable reverting to power on defaults	EF	CC
Disable release interrupt	EF	DD

The following symbols are used in the command descriptions.

Output registers

0	This indicates that the bit must be set to 0.
1	This indicates that the bit must be set to 1.
D	Indicates that the device number bit of the Device/Head Register should be specified. This bit is reserved This bit is reserved since all Serial ATA devices behave like Device 0 devices.
H	Head number. This indicates that the head number part of the Device/Head Register is an output parameter and should be specified.
L	LBA mode. This indicates the addressing mode. Zero specifies CHS mode and one specifies LBA addressing mode.
R	Retry. Original meaning is already obsolete, there is no difference between 0 and 1. (Using 0 is recommended for future compatibility.)
B	Option Bit. This indicates that the Option Bit of the Sector Count Register be specified. (This bit is used by Set Max ADDRESS command.)
V	Valid. This indicates that the bit is part of an output parameter and should be specified.
x	This indicates that the hex character is not used.
-	This indicates that the bit is not used.

Input registers

0	This indicates that the bit is always set to 0.
1	This indicates that the bit is always set to 1.
H	Head number. This indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.
V	Valid. This indicates that the bit is part of an input parameter and will be set by the device to 0 or 1.
N	Not recommended condition for start up. Indicates that the condition of the device is not recommended for start up.
-	This indicates that the bit is not part of an input parameter. Symbols are used in the command descriptions:

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

Please refer to ATA Interface spacification about another command's description which are not described in this SATA interface specification.

However, be careful that Serial ATA Device/Head register 4 bit (D) is different from ATA. In Serial ATA, Device/Head register 4 bit is reserved for all commands.

11.1 Identify Device (ECh)

Table 38: Identify Device command (ECh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 1 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Table 39 beginning on page 56.

Table 39: Identify device information (Part 1 of 7)

An asterisk (*) in next to the Content field indicates the use of those parameters that are vendor specific.

Word	Content		Description	
00	045AH or 045Eh		*drive classi-fication*	*bit assignments*
			15(=0)	1=ATAPI device, 0=ATA device
			14 - 8	retired
			7(=0)	1=removable cartridge drive
			6(=1)	1=fixed drive
			5 - 3	retired
			2(=0)	1=soft sectored
			1	retired
			0(=0)	Reserved
01	XXXXH		Number of cylinders in default translate mode	
02	37C8H		Specific Configuration 37C8H: Need Set Feature for spin-up after power-up Identify Device is incomplete	
03	00XXH		Number of heads in default translate mode	
04	0	*	Reserved	
05	0	*	Reserved	
06	003FH		Number of sectors per track in default translate mode	
07	0000H	*	Number of bytes in sector gap	
08	0000H	*	Number of bytes in sync field	
09	0000H	*	Reserved	
10-19	XXXX		Serial number in ASCII (0 = not specified)	
20	0003H	*	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read	
21	XXXXH	*	Buffer size in 512-byte increments	
22	0034H	*	Number of ECC bytes (Vendor unique length is selected via Set Feature Command)	
23-26	XXXX		Micro code version in ASCII	
27-46	XXXX		Model number in ASCII	
47	8010H		15-8: (=80h) 7-0: Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands.	

Table 40: Identify device information (Part 2 of 7)

An asterisk (*) in next to the Content field indicates the use of those parameters that are vendor specific

Word	Content		Description
48	0000H		Reserved
49	XF00H	*	Capabilities, bit assignments: 15-14(=0) Reserved 13 Standby timer (=1) Values as specified in ATA standard are supported (=0) Values are vendor specific 12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) Reserved 8(=0) Reserved 7-0(=0) Reserved
50	4000H		Capabilities. bit assignments 15-14(=01) Word 50 is valid 13- 1(=0) Reserved 0 Minimum value of Standby timer (=0) less than 5 minutes (=1) equal to or greater than 5 minutes
51	0200H		PIO data transfer cycle timing mode
52	0200H	*	DMA data transfer cycle timing mode. Refer to Word 62 and 63
53	0007H		Validity flag of the word 15- 3(=0) Reserved 2(=1) 1 Word 88 is Valid 1(=1) 1=Word 64-70 are Valid 0(=1) 1=Word 54-58 are Valid
54	XXXXH		Number of current cylinders
55	XXXXH		Number of current heads
56	XXXXH		Number of current sectors per track
57-58	XXXXH		Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH		Current Multiple setting. Bit assignments: 15- 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	XXXXH		Total Number of User Addressable Sectors Word 60 specifies the low word of the number FFFFFFFh=The 48-bit native max address is greater than 268,435,455
62	0000H		
63	XX07H		Multiword DMA Transfer Capability 15- 8 Multiword DMA transfer mode active 7- 0(=7) Multiword DMA transfer modes supported (support mode 0,1,and 2

Table 41: Identify device information (Part 3 of 7)

Word	Content	Description
64	0003H	Flow Control PIO Transfer Modes Supported 15- 8(=0) Reserved 7- 0(=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
67	00F0H	Minimum PIO Transfer Cycle Time Without Flow Control 15- 0(=F0h) Cycle time in nanoseconds (240 ns, 8.3 MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
69-74	0000H	Reserved
75	00XXH	Queue depth 15- 5 Reserved 4- 0 Maximum queue depth
76		SATA Generation
76-79	0000H	Reserved
80	007CH	Major version number 15- 0 (=7C) ATA-2,ATA-3,ATA/ATAPI-4,ATA/ATAPI-5,ATA/ATAPI-6
81	0019H	Minor version number 15- 0 (=19) ATA/ATAPI-6 T13 14100 Revision 3a
82	74EBH	Command set supported 15(=0) Reserved 14(=1) NOP command 13(=1) READ BUFFER command 12(=1) WRITE BUFFER command 11(=0) Reserved 10(=1) Host Protected Feature set 9(=0) DEVICE RESET command 8(=0) SERVICE interrupt 7(=1) RELEASE interrupt 6(=1) LOOK AHEAD 5(=1) WRITE CACHE 4(=0) PACKET Command Feature set 3(=1) Power Management Feature Set 2(=0) Removable feature set 1(=1) Security feature set 0(=1) SMART feature set

Table 42: Identify device information (Part 4 of 7)

Word	Content	Description
83	7BEAH	Command set supported 15-14 Word 83 is valid 13(=1) FLUSH CACHE EXT command supported 12(=1) FLUSH CACHE command supported 11(=1) Device Configuration Overlay command supported 10(=1) 48-bit Address Feature Set supported 9(=1) Automatic Acoustic mode 8(=1) SET Max Security extension 7(=1) Set Features Address Offset Feature mode 6(=1) SET FEATURES subcommand required to spin-up 5(=1) Power-Up In Standby feature set supported 4(=0) Removable Media Status Notification feature 3(=1) Advanced Power Management Feature Set 2(=0) CFA feature set 1(=1) READ/WRITE DMA QUEUED 0(=0) DOWNLOAD MICROCODE command
84	4000H	Command set/feature supported extension 15-14 Word 84 is valid 13- 2 Reserved
85	XXXXH	Command set/feature enabled 15 Reserved 14 NOP command 13 READ BUFFER command 12 WRITE BUFFER command 11 Reserved 10 Host Protected Area Feature Set 9 DEVICE RESET command 8 SERVICE interrupt 7 RELEASE interrupt 6 LOOK AHEAD 5 WRITE CACHE 4 PACKET Command Feature Set 3 Power Management Feature Set 2 Removable Feature Set 1 Security Feature Set 0 SMART Feature Set

Table 43: Identify device information (Part 5 of 7

Word	Content	Description
86	XXXXH	Command set supported 15-14 Reserved 13 FLUSH CACHE EXT command supported 12 FLUSH CACHE command supported 11 Device Configuration Overlay command supported 10 48-bit Address Feature Set supported 9 Automatic Acoustic Management enabled 8 SET Max Security extension enabled 7 Set Features Address Offset Feature mode 6 Set Features subcommand required to spin-up after power- up 5 Power-Up In Standby feature set enabled 4 Removable Media Status Notification feature 3 Advanced Power Management Feature Set 2 CFA feature set 1 READ/WRITE DMA QUEUED 0 DOWNLOAD MICROCODE command
87	4003H	Command set/feature enabled 15-14(=01) Word 87 is valid 13- 6(=0) Reserved 5(=1) General Purpose Logging feature set supported 4-2(=0) Reserved 1(=1) SMART self-test supported 0(=1) SMART error logging supported
88	0X3FH	Ultra DMA transfer modes 15- 8(=xx Current active Ultra DMA transfer mode 15-14 Reserved (=0) 13 Mode 5 1=Active 0=Not Active 12 Mode 4 1=Active 0=Not Active 11 Mode 3 1=Active 0=Not Active 10 Mode 2 1=Active 0=Not Active 9 Mode 1 1=Active 0=Not Active 8 Mode 0 1=Active 0=Not Active 7- 0(=3F) Ultra DMA transfer mode supported 5 Mode 5 1=Support 4 Mode 4 1=Support 3 Mode 3 1=Support 2 Mode 2 1=Support 1 Mode 1 1=Support 0 Mode 0 1=Support
89	XXXXH	Time required for Security Erase Unit completion Time= value x 2 [minutes]
90	0000H	Time required for Enhanced Security Erase completion
91	0000H	Current Advanced Power Management value
92	FFFEH	Master Password Revision Code

Table 44: Identify device information (Part 6 of 7)

Word	Content	Description
93	0000H	(=0) COMRESET result
94	XXXXH	Current Automatic Acoustic Management value Vendor's Recommended Acoustic Management level 15-8 Current Acoustic Management level
95-99	0000H	Reserved
100-103	xxxxH	Minimum user LBA address for 48-bit Address feature set
104-126	0000H	Reserved
127	0000H	Removable Media Status Notification feature set 0000H = Not supported
128	XXXXH	Security Mode Feature. Bit assignments 15-9 Reserved 8 Security Level: 1= Maximum, 0= High 7-6 Reserved 5 Enhanced erase 1= Support 4 Expire 1= Expired 3 Freeze 1= Frozen 2 Lock 1= Locked 1 Enable/Disable 1= Enable 0 Capability 1= Support

Table 45: Identify device information (Part 7 of 7)

An asterisk (*) in next to the Content field indicates the use of those parameters that are vendor specific

Word	Content		Description
129	XXXXH	*	Current Set Feature Option. Bit assignments 15-4 Reserve 3 Auto reassign 1= enabled 2 Reverting 1= enabled 1 Read Look-ahead 1= enabled 0 Write Cache 1= enabled
130-159	XXXXH	*	Reserved
160-254	0000H	*	Reserved
255	XXA5H		15- 8 Checksum. This value is the two’s complement of the sum of all bytes in byte 0 through 510 7- 0 Signature

11.2 Read Long (22h/23h)

Table 46: Read Long (22h/23h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	- - - - - - - V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 0 0 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media. It then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 40 according to the setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 8–15 (Low), 16–23 (High). (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 24–27. (L = 1)

R This indicates the retry bit. This bit is ignored.

Feature ECC count

Input parameters from the device

Sector Count	This indicates the number of requested sectors not transferred
Sector Number	This indicates the sector number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 0–7. (L = 1)
Cylinder High/Low	This indicates the cylinder number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 8–15 (Low), 16–23 (High). (L = 1)
H	This indicates the head number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 24–27. (L = 1)

11.3 Write Long (32h/33h)

Table 47: Write Long (32h/33h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	- - - - - - - V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 1 0 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are either 4 or 40 according to setting of the Set Feature option. The default number after power on is 4 bytes.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High) (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 24–27. (L = 1)

R The retry bit. This bit is ignored.

Feature ECC count

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)
In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low	This indicates the cylinder number of the sector to be transferred. (L = 0) In LBA mode this register contains current the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the sector to be transferred. (L = 0) In LBA mode this register contains current the LBA bits 24–27. (L = 1)

12.0 Timings

The timing of BSY and DRQ in Status Register are shown in the table below.

Table 48: Time-out values

FUNCTION	INTERVAL	START	STOP	TIME-OUT
Power On and COMRESET Device Busy After Power On	Devince Ready After Power On	COMRESET	The Device sets BSY (=0) and RDY (=1) to the Register and requests to send the Register FIS to the Host.	31 sec
Software Reset	Device Busy After Software Reset	The Host asserts SRST(=1) to the Device Control Register and send the Register FIS to the Device.	The Host Adapter sets BSY(=1) to the Status Register.	400 ns
	Device Ready After Software Reset	The Host asserts SRST(=1) to the Device Control Register and send the Register FIS to the Device. Then the Host negates SRST(=0) to the Device Control Register and send the Register FIS to the Device.	The Device sets BSY(=0) and RDY(=1) to the Status Register and requests to send the Register FIS to the Host.	31 sec
COMRESET	Device Ready After COMRESET	COMRESET Signal Asserted	The Device sets BSY (=0) and RDY (=1) to the Status Register and requests to send the Register FIS to the Host	31 sec
Non-Data Command	Device Busy After the register FIS for Command.	The host sets commands to Command Register and sends the Register FIS.	The Host Adapter sets BSY (=1) to the Status Register.	400 ns
	The Register FIS for Command Complete	The Host Adapter sets BSY (=1) to the Status Register.	The Device sets the status of command to the Status Register and requests to send the Register FIS to the Host.	30 sec

Command category is referred to in section 10.0, "Command protocol" on page 47.

The abbreviations "ns", "μs", "ms," and "sec" mean nanoseconds, microseconds, milliseconds, and seconds, respectively.

If the host detects a time-out while waiting for a response from the device, we recommend that the host system execute a Soft reset and then retry the command.

FUNCTION	INTERVAL	START	STOP	TIMEOUT
PIO Data In Command	Device Busy After the register FIS for Command.	The Host sets commands to Command Register and sends the Register FIS to the Device.	The Host Adapter sets BSY (=1) to the Status Register	400 ns
	PIO SETUP FIS for Data Transer In	The Host Adapter sets BSY (=1) to the Status Register	The Device sets BSY (=0) and DRQ (=1) to the Status Register and requests to send the PIO SETUP FIS to the Host.	30 sec
	Device Busy After Data Transfer In	The PIO SETUP FIS is transfered to the Host.	The Host Adapter sets BSY (=1) to the Status Register	400 ns
DMA Data Transfer Command	Device Busy After the Register FIS for Command.	The Host sets commands to Command Register and sends the Register FIS.	The Host Adapter sets BSY(=1) to the Status Register.	400 ns

Command category is referred to 11.0, "Command Protocol."
The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.
We recommend that the host system executes Soft reset and then retries to issue the command if the host system timeout would occur for the device.

Index

F

G

H

I

J

L

M

N

O

P

R

S

T

U

V

W

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